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| Name: Muhammad Aziz Haider | EE-272L Digital Systems Design |
| Reg. No: 2020-EE-172 | Marks Obtained: \_\_\_\_\_\_\_\_\_\_\_\_ |

**CEP Manual**

**Single Cycle RISC-V Processor for GCD**

**Truth Table for Controller**

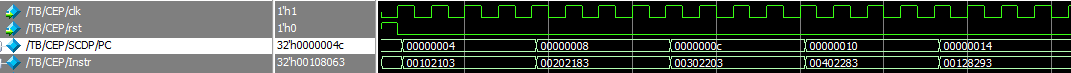
|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Instruction | opcode | RegWrite | ImmSrc | ALUSrc | ResultSrc | ALUOp |
| I-Type lw | 0000011 | 1 | 0 | 1 | 1 | 00 |
| I-Type addi | 0010011 | 1 | 0 | 1 | 0 | 10 |
| R–Type | 0110011 | 1 | X | 0 | 0 | 10 |
| B-Type | 1100011 | 0 | 1 | 0 | x | 01 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Instruction | ALUOp | func3 | RtypeSub = op[5] & func7[5] | ALUControl |
| lw | 00 | x | X | 000 |
| add - addi | 10 | 000 | 0 | 000 |
| sub | 10 | 000 | 1 | 001 |
| sltu | 10 | 000 | X | 101 |
| bne | 01 | X | X | 001 |
| beq | 01 | X | X | 001 |

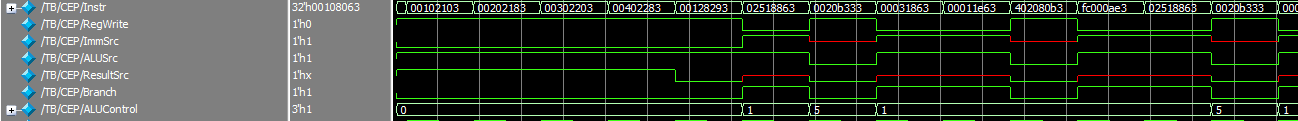
**Decreasing frequency of the clock**

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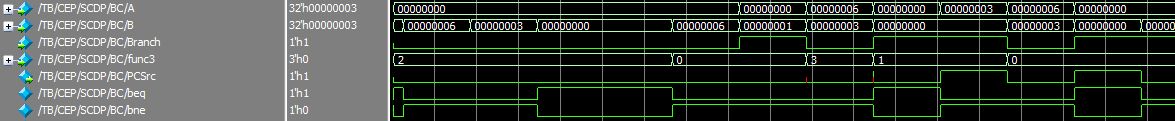
**Reading Instructions from Instruction Memory**

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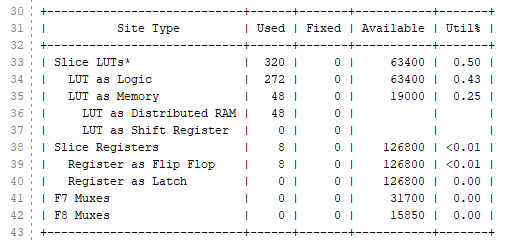
**Controller Signals**

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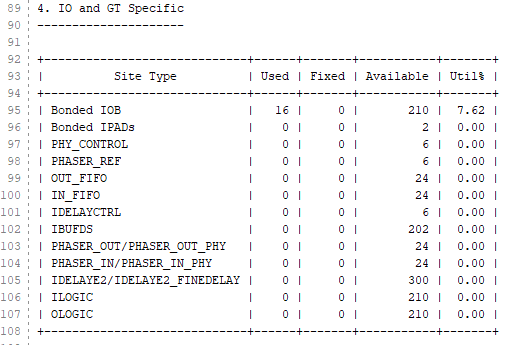
**Branch Comparator**

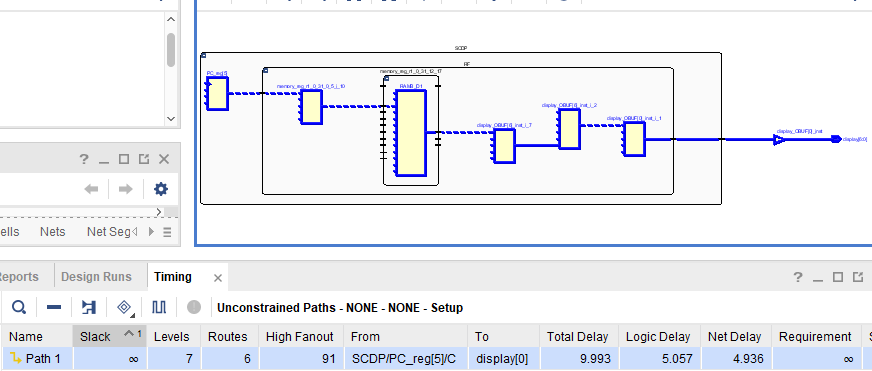
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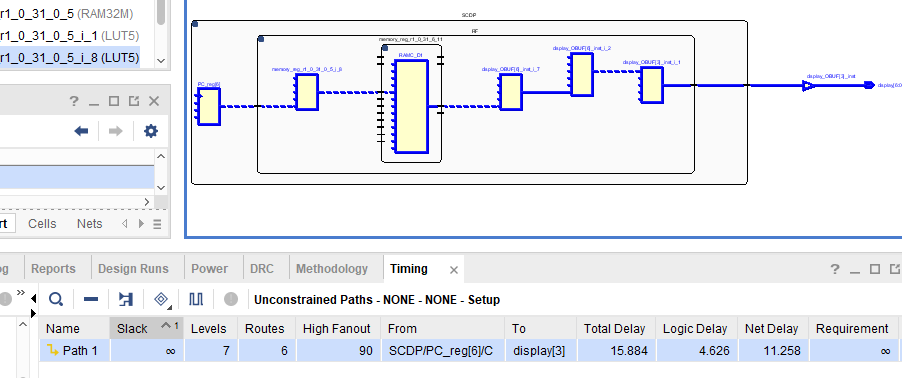
**LUTs Used**

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**I/O Specifics**

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**Pre Implementation Delay**

**Post Implementation Delay**